



# Integrating WireFlow modules with NI VeriStand

## Abstract

This application note describes two methods of integrating WireFlow C Series modules with NI VeriStand. The first method involves creating custom FPGA-based I/O personalities for NI VeriStand. The second method uses the NI VeriStand add-on called Scan Engine and EtherCAT custom device.

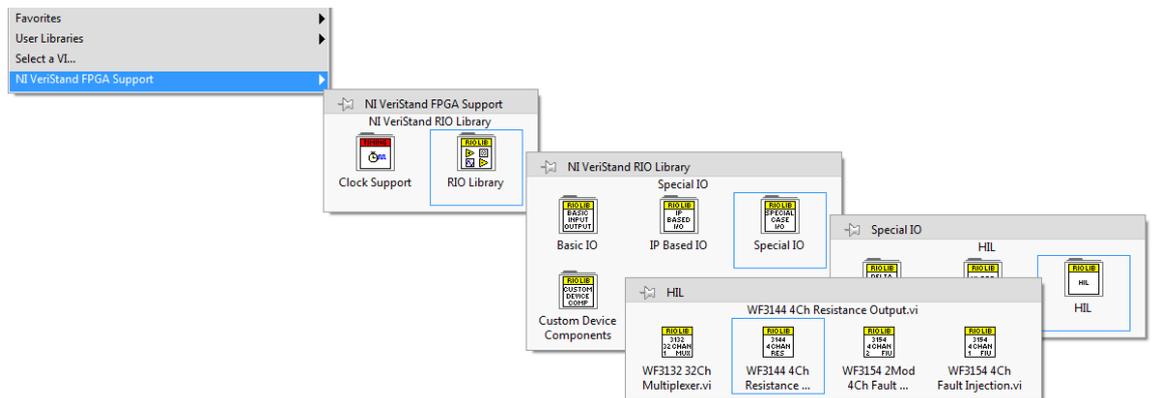
Example code is available as a zip file from [www.wireflow.se/downloads](http://www.wireflow.se/downloads) (AB0005-099 AN14 Integrating WF modules with NI VeriStand examples.zip).

## Method 1 - NI VeriStand FPGA Interface Tools

NI VeriStand ships with a variety of standard analog, digital, and communication bus interfaces. However, for you to be able to add user-defined I/O hardware, NI VeriStand provides the ability to create custom FPGA-based I/O personalities. The procedure of installing the toolkit and implementing personalities is described in detail in this article: <https://decibel.ni.com/content/docs/DOC-13815>. The article includes:

- A download link for the toolkit called NI VeriStand FPGA Interface Tools for LabVIEW
- Detailed guidelines on how to create and use custom I/O personalities
- Link to a white paper called Creating FPGA-Based I/O Personalities for NI VeriStand

Since version 1.3.0, the toolkit includes support for WireFlow C Series modules (WF 3144, WF 3154 and WF 3132) under the NI VeriStand RIO Library > Special IO > HIL palette.



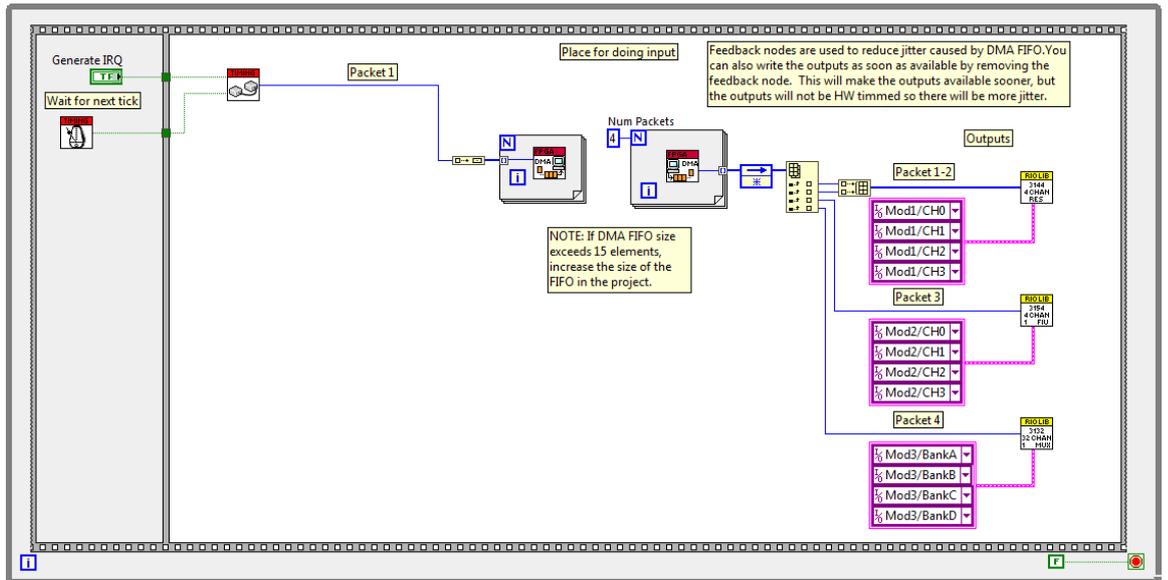
Here is an example where the WireFlow modules are added to the communications loop of the framework template.

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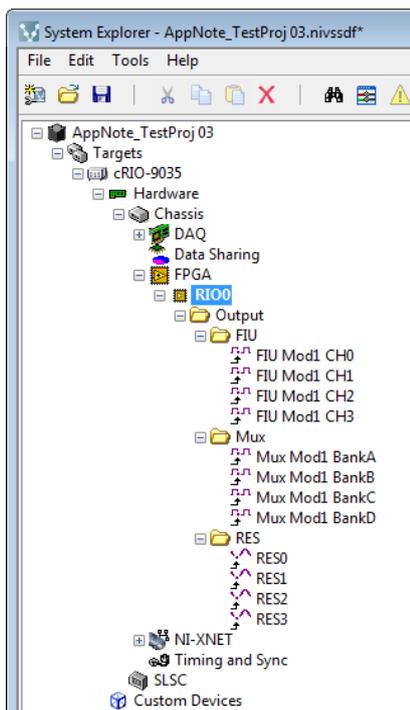
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This excerpt from the article summarizes the steps involved.

1. Customize the FPGA VI generated by the NI VeriStand Custom FPGA Project Wizard.
2. Compile the FPGA VI to generate the bitfile (.lvbitx)
3. Modify the FPGA config XML file (.fpgaconfig) to match the packet definition in the FPGA VI (RIO Library VIs have the XML on their block diagram)
4. Copy the bitfile, config XML file, and schema (.xsd) either to your NI VeriStand project directory or to the globally available Public Documents\National Instruments\- 5. Add the FPGA personality to an NI VeriStand System Definition

After completing the steps, the I/O channels are available in the NI VeriStand System Explorer under your controller > Hardware > Chassis > FPGA.



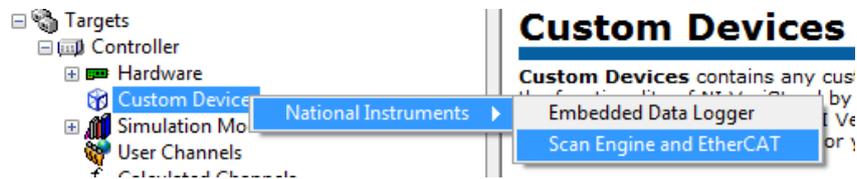


## Method 2 - Scan Engine and EtherCAT custom device

The Scan Engine and EtherCAT custom device allows users to easily read scanned I/O from C series modules located in a CompactRIO, NI 9144 or NI 9145 EtherCAT chassis. This NI VeriStand add-on is thoroughly described in this article: <https://forums.ni.com/t5/NI-VeriStand-Add-Ons-Documents/NI-VeriStand-Add-On-Scan-Engine-and-EtherCAT/tab/3514244>. Version 2018: <http://www.ni.com/download/ni-veristand-2018/7785/en/>.

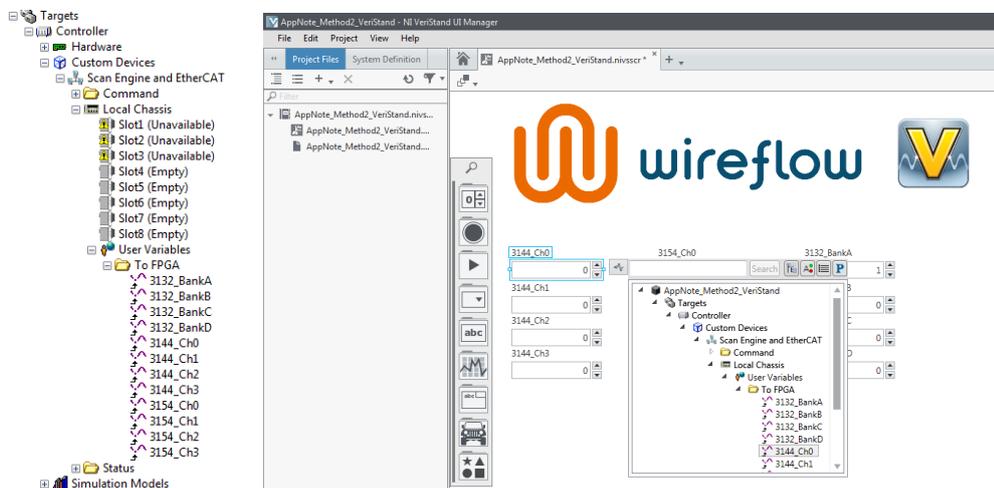
This solution takes advantage of the hybrid mode in which the WireFlow modules are in FPGA mode and the remaining modules are in scan mode. Although a custom FPGA bitfile must be built and downloaded, the remaining slots in the chassis are available for Scan Engine access to NI modules. It is even possible to switch between NI modules in the remaining slots without FPGA recompilation. User Defined Variables are used to control the channels of the WireFlow modules, and they behave just like the rest of your I/O.

1. Read more about mixing WireFlow and National Instruments modules, and study example code by downloading application note no. 4 (Mixing WF and NI Modules) from [www.wireflow.se/downloads](http://www.wireflow.se/downloads)
2. Create a LabVIEW project to access WireFlow modules by User Defined Variables, as described in application note no. 4
3. Compile the FPGA VI to generate the bitfile (.lvbitx)
4. Copy the bitfile either to your NI VeriStand project directory or to the globally available Public Documents\National Instruments\<NI VeriStand Version>\FPGA directory
5. In the NI VeriStand System Explorer under Targets > Controller > Hardware > Custom Device, right click and add Scan Engine and EtherCAT



6. Click Add Local Chassis
7. Select User Variables and click Select/Change FPGA Bitfile. Select your bitfile.

Here is an example where WF 3144, WF 3154 and WF 3132 channels are available in slot 1-3 via User Variables and where they are accessed in an NI VeriStand UI screen.



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