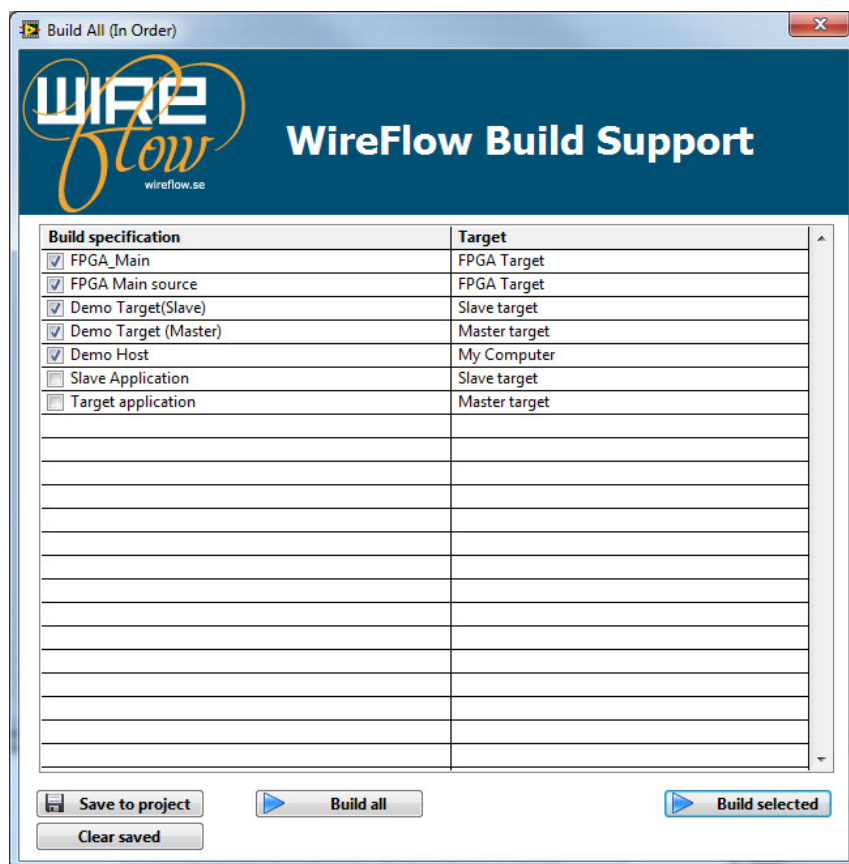




WireFlow Build Support User's Manual

AC0011-003 rev A



Contents

Support information	2
Technical support and Product information	2
WireFlow headquarters.....	2
Important information	2
End User Licence Agreement.....	2
Copyright	2
Introduction	3
Features	3
Details.....	5
Build in order... ..	5
Buttons	6
Zip Export.....	6
Preferences.....	7
Help	7
Example.....	8
Build all (in order) - Example.....	8
Troubleshooting	11
Technical support and Professional services.....	11
Appendix: EULA	12

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Please see appendix “Technical support and Services” for more information.

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Important information

End User Licence Agreement

Please read the EULA before installing or using this Software (**Appendix: EULA**).

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Introduction

The WireFlow Build Support adds the possibility to invoke builds across different targets and in a user specified order. The desired build order and the currently active build specifications can be saved in the project. This means that all users can build the project build specifications in exactly the same way.

In LabVIEW 2010 and later it is also possible to have FPGA build items specified in the build order, meaning that Windows/RealTime applications depending on FPGA builds, can be built with a single build action.

As an additional feature, it is also possible to easily create a zipped project development distribution (including the project file itself), not including the Program folder items.

Features

The “Application Builder Support” adds a number of new items to the LabVIEW project contextual menus.

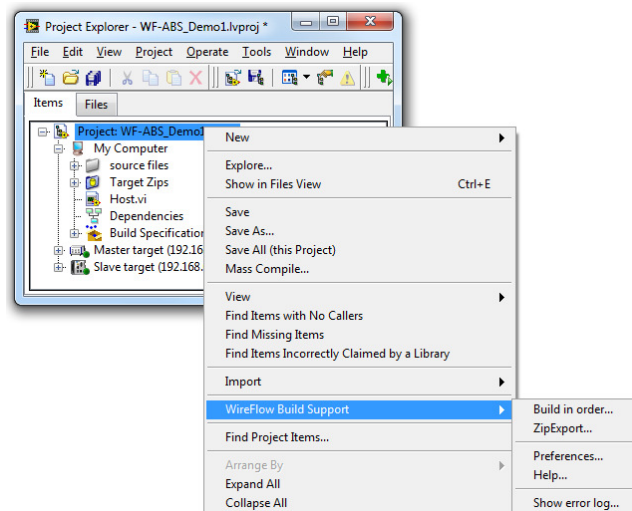











Figure 1. WireFlow Build Support contextual menu

Depending on which item that is right-clicked, one or more new items can be seen in a sub category called WireFlow Build Support (see Figure 1).

The main feature is the ability to execute builds in a predefined order, regardless of target, with a single menu selection. This is sort of a general **One-Click-Build** solution, enabling users to build all items in a project in a predefined order automatically, e.g. FPGA->RT->Windows.

The “Application Builder Support” actions that are included in the tool are listed in the table below (see Table 1). In Table 1, the second column specifies the project items where a specific action is available.

Table 1. Supported project actions

Action	Supported Project items	Description
Build in order...	 Root  Build Specifications	<p>Opens a configuration panel that lets the user define Build order by drag and drop, enable or disable builds by checking/unchecking builds.</p> <p>In addition the user can select to save the configuration in the project file, Build the selected items or Build all items currently in the project.</p>
ZipExport	 Root	<p>Only available on the root project item.</p> <p>Exports all linked project files (including the project file itself) to a zip file for easy delivery of source code.</p>
Preferences...	 Root  Build Specifications	Opens the Build Support preference dialog.
Help	 Root  Build Specifications	Opens this help document (in pdf format)
Show Error Log	 Root  Build Specifications	<p>Opens the error log file.</p> <p>This selection is only available if the error log exists</p>

Details

Build in order...

The "Build in order..." action opens a window displaying the detected build items.

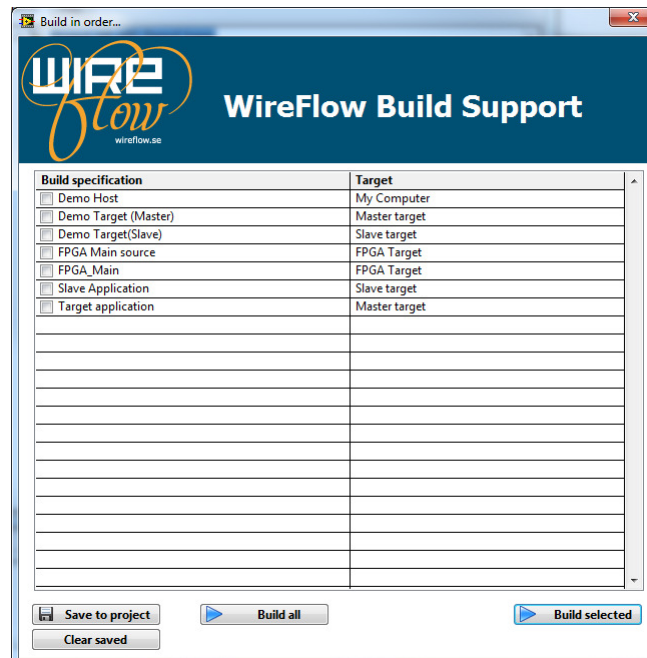


Figure 2. Build in order first launch.

First time the window is displayed it shows all available build configurations in the project, sorted by name, and no items are checked to be active (see Figure 2).

To change the build order just drag-n-drop the build items into the desired order, and check the items that should be built. The active items and the build order can be saved in the lvpjproj-file so that all users can use the same build order.

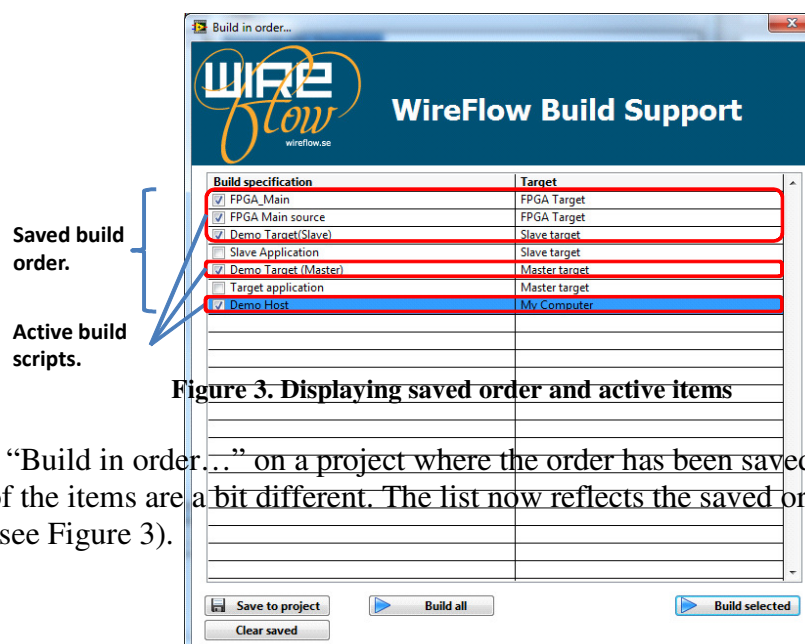


Figure 3. Displaying saved order and active items

When selecting "Build in order..." on a project where the order has been saved in the project file the listing of the items are a bit different. The list now reflects the saved order, with active items selected (see Figure 3).

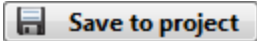
The build items are stored by name, and if the name of a target and/or build item is changed the “Build in order...” window will list these items with a specific symbol to indicate that the item was not found.

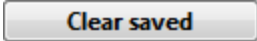
	Build specification	Target
Active build item	<input checked="" type="checkbox"/> FPGA_Main	FPGA Target
	<input checked="" type="checkbox"/> FPGA Main source	FPGA Target
Active but missing build item	<input checked="" type="checkbox"/> Demo Target(Slave)	Slave target
	<input checked="" type="checkbox"/> Demo Target (Master)	Master target
	<input checked="" type="checkbox"/> Demo Host	My Computer
Inactive build item	<input type="checkbox"/> Demo Target(Slave)	Slave target2
	<input type="checkbox"/> Slave Application	Slave target2
	<input type="checkbox"/> Target application	Master target

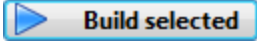
Figure 4. Listing items with different symbols.

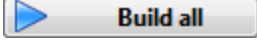
In Figure 4 the target name was changed from “SlaveTarget” to “SlaveTarget2”, and the save build item is therefore not found. These missing items will be removed automatically if the build order is saved to the project.

Buttons

- 

Save the current order to the project file, only active items will be saved. If missing items are present, these will automatically be removed.
Does not actually save the project itself.
- 

Clears the saved build information.
Does not actually save the project itself.
- 

Builds the selected build items in the specified order. The build progress will be displayed in a separate progress bar window.
- 

Builds all build items in the currently set order, i.e. discards the selection checkbox. The build progress will be displayed in a separate progress bar window.

On LabVIEW version 2010 and forward, the FPGA build will also be available

Zip Export

ZipExport is only available on the project root-object and offers the user a quick way of distributing files linked from the project.

The ZipExport function does not include items in the Program files folder.

Preferences

For each project it is possible to specify a number of settings related to how the different build items should be built.



Figure 5. Preferences dialog

- **Save project before builds?**
Some builds need to save the project file before building, e.g. if auto-populating folders are used. When this option is turned on, the build engine will automatically try to save the project file before each build steps is invoked.
- **Stop on build error?**
If set, the build engine will stop processing the build steps if an error is generated. Default is False, meaning that the builds will continue and all errors will be presented at the end.
- **Display Result dialog?**
If False the result dialog will only be displayed if one or more build steps generated error. If True the result dialog will always be displayed.
- **Wait for FPGA builds to complete.**
In LabVIEW > 2010 the module also support building LabVIEW FPGA builds, and this option allows the user to select if the build engine should wait for a FPGA compilation to complete before continuing to the next build item.

Help

Selecting help opens this help document in pdf-format

Example

Build all (in order) - Example

This example demonstrates the usage of the action “Build in order...”, and how that can be used to simplify the build process.

To start with we have a multi-target project; Windows, RT(Pharlap), RT(VXworks) and FPGA.

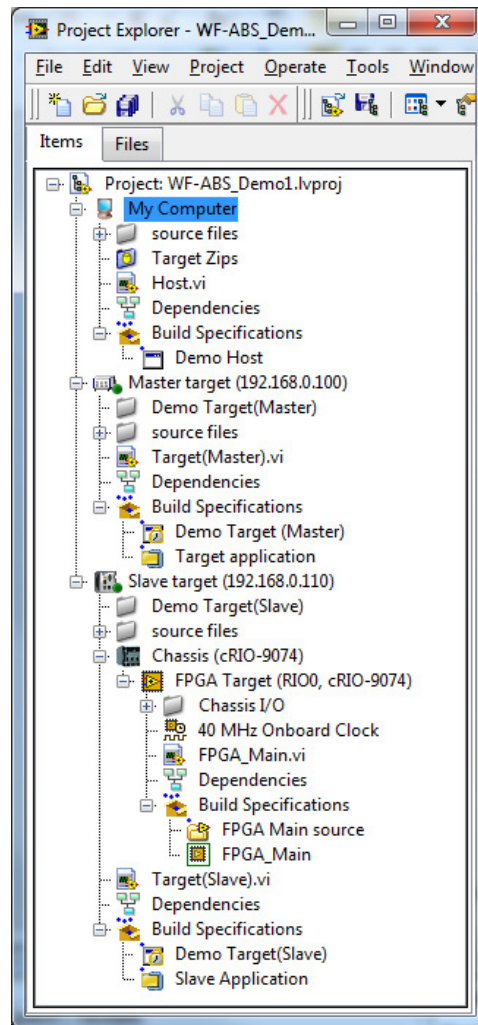


Figure 6. Example project

In order to make a complete build for this project for delivery, we have to build the items (in this order)

- FPGA Main (only available in LabVIEW > 2010)
- FPGA Main Source
- Demo Target(Slave)
- Slave Application
- Demo Target(Master)
- Target Application
- Demo Host

We can go through all these builds one-by-one manually, but then we risk that the user builds in the wrong order or forget one or more builds. It also takes some time to sit and wait for all the builds to finish.

This is where the WireFlow build support comes in. Once we invoked the “Build in order...” action we drag the builds in the order we want them to be invoked.

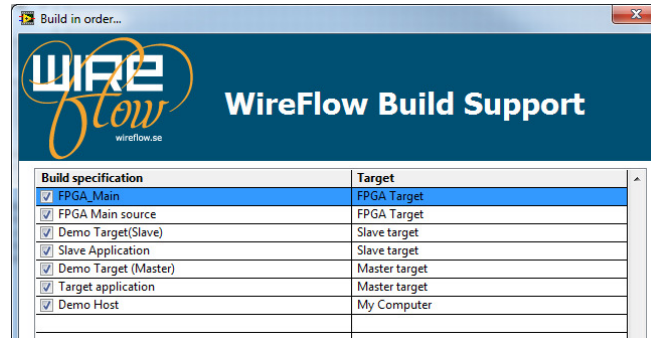
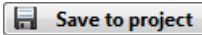
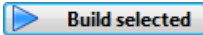


Figure 7. Build order defined in the example project.

Then when we have set the order as expected (see Figure 7), we can either choose  or . If we want the order to be saved for the next time should “Save to project” before selecting “Build selected”.

When “Build selected” is pressed the build engine loads the project into memory and starts working on all the build steps.

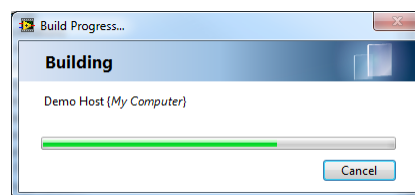


Figure 8. Build progress display.

If any build item generates an error, or if the preference “Display Result dialog?” is TRUE, a result dialog will be displayed.

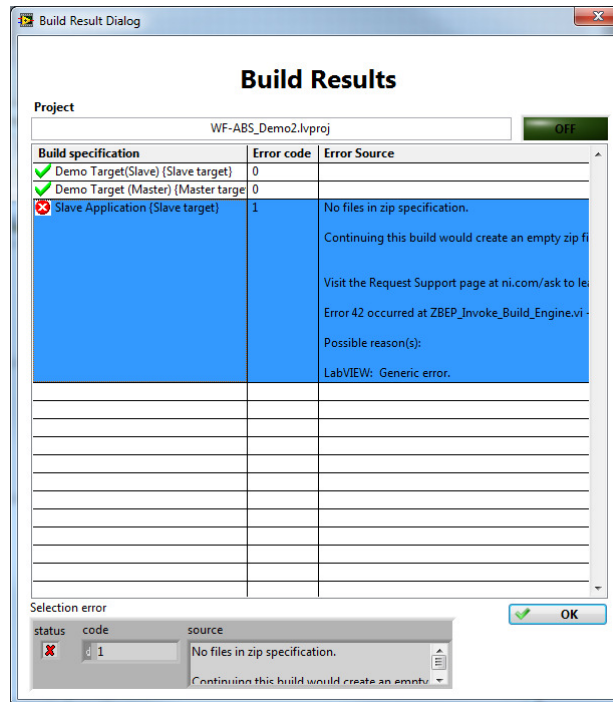


Figure 9. Result dialog

Selecting an error in the result list will present the error in the Error cluster in the lower part so that you can select explain error.

Troubleshooting

After installation with VIPM it is necessary to restart LabVIEW to get this provider correctly loaded.

In order to use the “Save before build option”, it is necessary that the lvproj file is not write protected.

LabVIEW FPGA builds are only supported on LabVIEW 2010 and higher.

Technical support and Professional services

The most recent version of this software will be available as a VIPM package at www.wireflow.se, and also published to the LabVIEW Tool Network.

Please direct any support questions to support@wireflow.se, and in the case of an error please attach the error log file and a description of the problem as detailed as possible.

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