Using WireFlow C Series modules in Scan Mode

Abstract

The NI-DAQ platform is currently closed for almost all third-party C Series modules, the WireFlow WF-3132 multiplexer module being one of the exceptions. This document shows how users that don't have access to NI-FPGA, still can use the WireFlow C Series modules in their systems.

The solution in this case is to use a RIO expansion chassis, and a pre-compiled FPGA bitfile. Here we use a NI-9146 Ethernet RIO expansion chassis as an example (pre-compiled bitfiles and LabVIEW projects can be downloaded from www.wireflow.se.

Introduction

Using DAQmx or Scan Engine is very convenient as a single type of driver can be used to communicate with almost any type of NI module. When it comes to third party modules, it is not as easy; DAQmx is a completely closed platform, except for a few modules like the WireFlow WF 3132 multiplexer module. And, third-party modules are not directly supported in ScanMode.

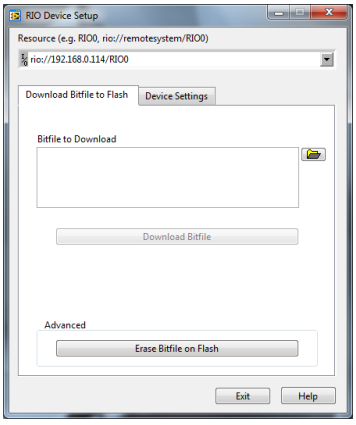
It is also a common misunderstanding that the LabVIEW FPGA module is needed to use a third-party module, and this together with the cost to buy the LabVIEW FPGA module sometimes steers users away from third party modules.

But this is not the case since third party developers can distribute pre-compiled bitfiles that allows the third-party module to co-exist with other standard NI C Series modules, given a specific slot for the third-party module.

The LabVIEW FPGA module is only needed if the configuration doesn't match the requirements, or if the FPGA is needed for the functionality of the other modules.

Deploying bitfiles to FPGA

To download FPGA bitfiles to a RIO device, we have to install the NI-RIO software that installs a specific application called "RIO Device Setup".



1. Open the "RIO Device Setup" application
2. Specify RIO resource to use (must be the same as the compile target)
3. Select bitfile to be deployed (bitfile should be compiled with "Run when loaded to FPGA" activated)
4. Press "Download bitfile"

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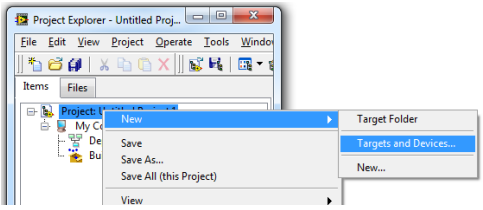
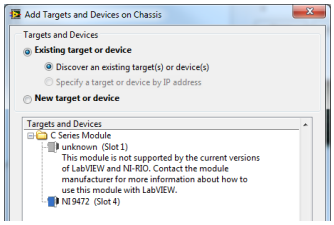
Application note no. 13
AB0005-041, rev C

Accessing the Module I/O

In this case we will use NI-9146 chassis configured with a WF-3144 module in the first slot and a NI-9132 in precompiled bitfile with a WireFlow WF3144 module in the first slot, and slot 0To get access to the variables from LabVIEW we first add the NI-9146 chassis a new target.



Right click on the chassis and select "New-> C Series Modules...".



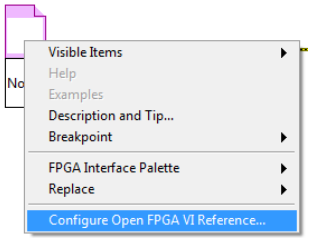
Let LabVIEW discover the modules (ignore the warning about the unknown module in slot 1 as this is the third-party module supported).

Then add a new VI under My Computer. In this VI we add the following functions from the FGPA interface palette:

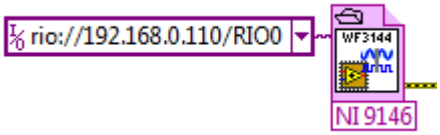
- Open FPGA VI reference
- Read/Write control
- Close FPGA VI reference

Right-click on the "Open FPGA VI reference" and select "Configure Open FPGA VI Reference...".

In the dialog we specify the Bitfile supplied by the third party developer, and make sure that "Run the FPGA VI is checked.



Next close the dialog and specify the FPGA resource by IP and name.



If the VI is correctly compiled, the Read/Write node will show the controls and indicators that can be accessed.

Finally we create our application using a mixture of ScanEngine access to NI native module and FPGA Read/Write access for the third party module.

Links

http://digital.ni.com/public.nsf/allkb/BAAA6D86CDDD583C8625729E00572C8B

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